



National University of Sciences and Technology

Military College of Signals

A course on

“FPGA based Chip Design”

13th March - 24th April 2010

Contents

- ★ Design and Tool Flow: Stages of ASIC/FPGA design
- ★ Verilog HDL Syntax and Semantics
- ★ Gateway Level Modeling
- ★ Verilog Operators
- ★ Verilog Behavioral Modeling
- ★ Timing Control
- ★ Writing Test Benches
- ★ Modeling Memories and FSM
- ★ Synthesis Tutorial

Registration Fee

UG Students*:

Rs.1000/-

PG students*/Faculty/Professionals/Other: Rs.2000/-

* Limited free seats for students with CGPA 3.6 and above

For Registration Contact:

Dr. Abdul Ghafoor

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Email: fpgaworkshop@mcs.edu.pk

Timings: 10:00-12:00 am

Days: Saturday 13th Mar, 20th Mar 2010

Friday 26th Mar 2010

Saturday 10th April, 24th April 2010

Venue: Military College of Signals,
Humayoun Road, Rawalpindi

Trainer: **Engr. Fayaz Hussain Gillani**

He has over 30 year experience in chip designing in military and commercial environment. Currently he is associated with AND OR Logic Pvt. Ltd.

Registration will be on first come first serve basis
(Deadline for registration 10 March 2010)